ABSTRACT

[0071] A logic block in a field programmable gate array comprises a plurality of clusters of logic devices. At least one of the logic devices in each of the clusters has an input or an output. A first set of interconnect conductors enters the logic block from a first side and forming a programmable intersection with the input or the output of at least one of the logic devices in each of the clusters. A second set of interconnect conductors enters the logic block from a second side and forming a programmable intersection with the input or output of one of the logic devices in each cluster, the first set of interconnect conductors forming a pairwise hardwired connection with the second set of interconnect conductors. An interconnect conductor splitting extension is disposed between the first set of interconnect conductors and the second set of interconnect conductors.